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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Marc Tremblay		
Title:	GROUPING LOGIC CIRCUIT IN A PIPELINED SUPERSCALAR PROCESSOR		
Application No.:	09/583,097	Filed:	August 2, 1999
Examiner:	E. Chan	Group Art Unit:	2183
Atty. Docket No.:	004-1391-1 (formerly SP-1391-2C US)		

July 18, 2002

COMMISSIONER FOR PATENTS
Washington, DC 20231

PRELIMINARY AMENDMENT

Claims 1-8 are pending. Prior to the first action on the merits, please amend the above-identified application as follows:

In the Specification

Please amend the specification to insert on page 1, before line 3, the following:

B1

This application is a continuation of Application No. 08/662,582, filed June 11, 1996, now U.S. Patent 5,958,042.

In the Claims

Please cancel claims 1-8 without prejudice or disclaimer to the subject matter recited therein. Please add the following new claims:

B2 Sub C8

9. A superscalar processor that performs, over plural execution cycles of the superscalar processor, instruction grouping for dispatch, including both intra-group and inter-group dependency checking.